ABSTRACT OF THE DISCLOSURE

In a level shifter, in the case where the amplitude voltage of an input signal (i.e., a first power voltage VDDL) input to an input terminal is changed to be higher and the amplitude voltage of an output signal (i.e., a second power voltage VDDH) output from an output terminal is changed to be lower, a fall delay time of the signal output from the output terminal tends to be longer than a rise delay time of the signal. However, an inverted input signal obtained by an inverter is input to a level shifting unit and also to the gate of an N-type transistor, and therefore, the N-type transistor is turned on at the fall of the input signal input to the input terminal, so as to supply a current based on the second power voltage VDDH to an output node of the level shifting unit for assisting the shift into H level performed in the level shifting unit. Accordingly, even when at least one of the amplitude voltage of the input signal and the amplitude voltage of the output signal is changed, balance between the fall delay time characteristic and the rise delay time characteristic of the output signal can be satisfactorily kept.